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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,905	10/22/2003	Jeffrey C. Tang	200304375-2	6559

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,905	TANG ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,11-15,17,19 and 22* is/are pending in the application.

4a) Of the above claim(s) *17,19 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-7 and 11-15, drawn to a double docking station with hot docking capability, classified in class 710, subclass 304.

   II. Amended claims 17, 19, and 22, drawn to a configuration for a network peripheral device in a docking station, classified in class 710, subclass 302.

2. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as connecting the portable computer to additional peripheral devices, and invention II has separate utility such as configuring a network device, wherein the device has a first part located at the portable computer and a second part located at the docking station. See MPEP § 806.05(d).

3. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 17, 19, and 22 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

4. Claims 11-12 are objected to because of the following informalities: Claims 11-12 are depending on the cancelled claim 10. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagisawa et al. (U.S. Patent No. 5,805,412).

Referring to claim 1: Yanagisawa discloses a CPU (figure 13, structure 11), a system memory (figure 13, structure 18), a bridge logic (figure 13, structure 22), and a control logic (figure 13, combined structures of 22, 23, and 30). Yanagisawa discloses a peripheral bus (figure 13, structures 17, 35, and the bus between structures 22 and 130) coupled to the bridge logic and an interface connector (figure 13, structure 130). Yanagisawa discloses an expansion device (figure 13, structure 200) with at least one storage device (column 14, line 18, Floppy Disk Drive), which is the claimed expansion device with drive wedge. Yanagisawa discloses that the control logic receiving docking station input signal (column 12, lines 64-67, column 13, lines 1-14). Yanagisawa discloses the hot docking capability (column 14, line 44). Yanagisawa further discloses a second docking unit (figure 14, structure 300) providing connections to

various peripheral devices and having an electrical connector (figure 14, structure 321) to the drive wedge. Yanagisawa's second docking unit is the claimed port replicator. Yanagisawa's second docking station providing the attached input signal to the control logic via the drive wedge (figure 13, structure 200). Yanagisawa's second docking station includes the media bay for storing information to be sent to the docked computer's the control logic (figure 13, combined structures of 22, 23, and 30) via the expansion device (figure 13, structure 200); thus, Yanagisawa discloses that the control logic detects a transition in the port replicator. Hence, claim is anticipated by Yanagisawa.

Referring to claim 11: Since Yanagisawa's control logic (figure 13, combined structures of 22, 23, and 30) enables the bus extended to the attached docking unit, Yanagisawa's control unit determines that the computer has been docked.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2-7 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yanagisawa and Ma et al. (U.S. Patent No. 5,875,307).

Referring to claim 2: Yanagisawa's disclosure is stated above. Although Yanagisawa discloses that the bridge does include a programmable interrupt controller (column 12, lines 21-22), Yanagisawa does not explicitly disclose the system management interrupt (SMI) and the sequence of events in response to the docking request. Ma discloses a method for managing hot docking/undocking. Ma's invention teaches a method for hot docking with the docking sequences completely transparent to the users. Ma discloses a sequence of events for each docking and undocking request (figures 3 and 4), and Ma's sequence discloses that the system controller issues a SMI for system reconfiguration (figure 3, steps 380 and 390). Ma teaches a method to eliminate the performance limitation and user limitation from the conventional practice, which may cause data loss or system damage (column 1, lines 60-61).

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Ma's teaching onto Yanagisawa at the time Applicant made the invention because Ma teaches one to prevent any data loss and system damage from docking/undocking by automatically conducting a sequence of specific transparent events.

Referring to claim 3: Ma discloses that the docking process may take place whether expansion unit is powered-on or powered-off (column 3, lines 50-52); thus, Ma implicitly discloses that the expansion unit has a power switch. Ma's expansion unit is equivalent to the expansion device.

Referring to claim 4: Ma discloses asserting an interrupt to CPU (figure 3, steps 380 and 390).

Referring to claim 5: Ma discloses reconfiguring the system upon detecting the docking (figure 3, step 390), which is equivalent to the claimed CPU directing bridge logic device to enable data bus when receiving interrupt signal from the bridge logic device.

Referring to claim 6: Ma discloses the SMI (figure 3, steps 380 and 390).

Referring to claim 7: Yanagisawa discloses an expansion device (figure 13, structure 200) with a floppy disk drive (column 14, line 18), which is an IDE device.

Referring to claim 12: Yanagisawa's disclosure is stated above. Although Yanagisawa discloses that the bridge does include a programmable interrupt controller (column 12, lines 21-22), Yanagisawa does not explicitly disclose the system management interrupt (SMI) and the sequence of events in response to the docking request. Ma discloses a method for managing hot docking/undocking. Ma's invention teaches a method for hot docking with the docking sequences completely transparent to the users. Ma discloses a sequence of events for each docking and undocking request (figures 3 and 4), and Ma's sequence discloses that the system controller issues a SMI for system reconfiguration (figure 3, steps 380 and 390). Ma teaches a method to eliminate the performance limitation and user limitation from the conventional practice, which may cause data loss or system damage (column 1, lines 60-61).

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Ma's teaching onto Yanagisawa at the time Applicant made the invention because Ma teaches one to prevent any data loss and system damage from docking/undocking by automatically conducting a sequence of specific transparent events.

Referring to claim 13: Yanagisawa discloses a CPU (figure 13, structure 11), a host bridge (figure 13, structure 14), a secondary bridge (figure 13, structure 22), and control logic (figure 13, combined structures of 22, 23, and 30). Yanagisawa discloses that the control logic receiving docking station input signal (column 12, lines 64-67, column 13, lines 1-14), which is equivalent to the claimed WEDGED# input signal. Yanagisawa discloses the hot docking capability (column 14, line 44). Yanagisawa further discloses a second docking unit (figure 14, structure 300) providing connections to various peripheral devices and having an electrical connector (figure 14, structure 321) to the expansion device (figure 13, structure 200). Yanagisawa's second docking station providing the attached input signal to the control logic via the expansion device (figure 13, structure 200); the attached input signal is equivalent to the claimed PRATTACHED# input signal. Yanagisawa's second docking unit is the claimed port replicator. Yanagisawa's control logic's means to received the docking signal is equivalent to the claimed pull-up resistor.

Although Yanagisawa discloses that the bridge does include a programmable interrupt controller (column 12, lines 21-22), Yanagisawa does not explicitly disclose the system management interrupt (SMI) and the sequence of events in response to the docking request. Ma discloses a method for managing hot docking/undocking. Ma's invention teaches a method for hot docking with the docking sequences completely transparent to the users. Ma discloses a sequence of events for each docking and undocking request (figures 3 and 4), and Ma's sequence discloses that the system controller issues a SMI for system reconfiguration (figure 3, steps 380 and 390). Ma teaches a method to eliminate the performance limitation and user limitation from the conventional practice, which may cause data loss or system damage (column 1, lines 60-61).

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Ma's teaching onto Yanagisawa at the time Applicant made the invention because Ma teaches one to prevent any data loss and system damage from docking/undocking by automatically conducting a sequence of specific transparent events.

Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Ma's teaching onto Yanagisawa at the time Applicant made the invention because Ma teaches one to prevent any data loss and system damage from docking/undocking by automatically conducting a sequence of specific transparent events.

Referring to claim 14: Ma discloses that the docking process may take place whether expansion unit is powered-on or powered-off (column 3, lines 50-52); thus, Ma implicitly discloses that the expansion unit has a power switch. Ma's expansion unit is equivalent to the expansion device.

Referring to claim 15: Yanagisawa discloses a keyboard control (figure 13, structure 26).

Response to Arguments

10. Applicant's arguments with respect to claims 1-7 and 11-15 have been considered but are moot in view of the new ground(s) of rejection stated above.

Allowable Subject Matter

11. Examiner withdraws the allowable subject matter stated in the previous Office Action dated 12/23/04.

Conclusion

12. The prior art made of recorded and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,035,354 to Klein: Klein discloses a CPU (figure 2, structure 56), a host bridge (figure 2, structure 64), a secondary bridge (figure 2, structure 70), and a control logic (figure 2, structure 78). Klein discloses that the control logic receives the docking station input signal (figure 2, column 4, lines 14-18); the docking input signal is equivalent to either WEDGED# signal or PRATTACHED# signal. Klein discloses a resistor (figure 2, structure 82). Klein discloses code executed by the CPU (figure 2, SMI).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
March 30, 2005

TIM VO
PRIMARY EXAMINER